REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

Disposition of Claims

Claims 1-19 were pending in the present application. By way of this reply, new claim 20 has been added. Accordingly, claims 1-20 are now pending in the present application. Claims 1, 6, 12, and 17 are independent. The remaining claims depend, directly or indirectly, from claims 1, 6, 12, and 17.

Claim Amendments

Independent claim 1 has been amended to clarify that the present invention is directed to a computer system with a reconfiguration module for determining an optimal configuration of cache memory for a particular application. Independent claim 6 has been amended to clarify that the present invention is directed to a method for determining an optimal configuration of cache memory for a particular application. Independent claim 12 has been amended to clarify that the present invention is directed to a computer system with a means for determining an optimal configuration of cache memory for a particular application. Independent claim 17 has been amended to clarify that the present invention is directed to a computer system with a reconfiguration module for determining an optimal configuration of a field-programmable gate array for a particular application.

No new matter has been added by way of these amendments as support for these amendments may be found, for example, in paragraphs [0022]-[0026] of the present application. Dependent claims 2-5, 7-10, 13-16, 18, and 19 have been correspondingly amended. Further,

independent claims 1 and 17 have been amended to correct minor grammatical errors and dependent claims 13-16 have been amended to depend directly or indirectly from independent claim 12. No new matter has been added by way of these amendments.

New Claim

By way of this reply, new claim 20 has been added to be dependent from independent claim 1. No new matter has been added by way of new claim 20 as support for this claim may be found, for example, in paragraph [0022] of the present application.

Abstract

The abstract has been amended to correct minor grammatical errors. Further, the abstract has been amended to more clearly indicate the claimed invention. No new matter has been added by way of these amendments.

Specification

A new title was required that clearly indicates the invention to which the claims are directed. By way of this reply, the title has been amended to better describe the present invention. Accordingly, withdrawal of any objection to the title is respectfully requested.

Paragraphs [0009]-[0012] corresponding to the Summary of the present application have been amended to be consistent with the independent claims of the present application. No new matter has been added by way of these amendments.

Additionally, paragraphs [0022] and [0025] of the present application have been amended to correct typographical errors. No new matter has been added by way of these amendments.

Rejection(s) under 35 U.S.C § 102

Claims 1-19 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent Application Publication No. 2002/0072893 in the name of Wilson (hereinafter "Wilson"). Independent claims 1, 6, 12, and 17 have been amended to clarify the present invention. To the extent that this rejection may still apply to the amended claims, this rejection is respectfully traversed.

The present invention is directed to a computer system having a reconfigurable cache memory. Such architecture allows cache memory to be reconfigured based on specific requirements for optimal performance (*see, e.g.*, paragraph [0021] of the present application).

Figure 4 of the present application shows a system **100** in accordance with an embodiment of the present invention. The system **100** has a functional unit **102**, a programmable memory unit **104**, and a reconfiguration unit **106**. The programmable memory unit **104** serves as necessary cache memory and may be a device such as a field programmable gate array (FPGA) (*see, e.g.*, paragraph [0022] of the present application). Performance information that is collected for a particular application may be used to determine the optimal cache memory configuration for that application (*see, e.g.*, paragraph [0023] of the present application). The reconfiguration unit **106** uses a vector representing the optimal cache memory configuration for a particular application to configure the programmable memory module **104** for that application (*see, e.g.*, paragraph [0023] of the present application).

Accordingly, independent claim 1 requires a reconfiguration module for determining an optimal configuration of cache memory for a particular application and programming the cache memory to the optimal configuration. Independent claim 6 requires determining an optimal configuration of cache memory for a particular application and programming the cache memory to the optimal configuration. Independent claim 12 requires a means for determining an

optimal configuration of cache memory for a particular application and programming the cache memory to the optimal configuration. Independent claim 17 requires a computer system with a reconfiguration module for determining an optimal configuration of a field-programmable gate array for a particular application.

Wilson, in contrast to the present invention, fails to disclose at least the limitations of independent claims 1, 6, 12, and 17 of the present application discussed above. Wilson discloses hardware emulations of microprocessor cores, or instruction sets, for testing and verification purposes (*see* Wilson, paragraphs [0003], [0006]). Wilson provides a processor core that executes subsets of an instruction to test and verify a microprocessor core that is soon to be manufactured. Additionally, Wilson emulates microprocessor cores with hardware in programmable logic devices such as FPGAs (*see* Wilson, paragraphs [0035] - [0036]). However, Wilson is completely silent with respect to reconfiguring a cache memory with an optimal configuration for a particular application that is to be executed. In fact, Wilson completely fails to contemplate the use of a reconfigurable cache memory as otherwise required by the claimed invention.

Wilson further notes that the ability for in-system reprogramming of an FPGA may be desirable in particular applications. As Wilson notes, the configuration memory of an FPGA is inherently reprogrammable (*see* Wilson, paragraphs [0050] - [0051]). However, Wilson is merely describing desirable properties of an FPGA for the particular application noted. That is, to be configurable for emulating a particular microprocessor core. Wilson states that the FPGA is at least once-programmable for defining user-provided configuration instructions (*see* Wilson, paragraphs [0040]-[0041], [0048]). Wilson is completely silent with respect to configuring a cache memory of a computer system dependent on optimal configuration information for a particular application.

Wilson additionally states that the microprocessor core emulator may have a hardware/software codesign system which allows specific functionality to be customized for hardware or software that is emulated according to the function partitioned to the hardware or software (*see* Wilson, paragraph [0197]). Elements such as software compilers, hardware compilers, and synthesizers for converting a register transfer level description to a net list may be parts of the system. This system creates partitions of functionality for a target system, so that parameters such as size and power of the hardware or software can be varied (see Wilson, paragraph [0205] - [0210]). However, Wilson is completely silent with respect to a method or apparatus for programming a cache memory to an optimal configuration of cache memory for a particular application as required by independent claims 1, 6, 12, and 17 of the present application.

In view of the above, Wilson fails to show or suggest the present invention as recited in amended independent claims 1, 6, 12, and 17. Thus, amended independent claims 1, 6, 12, and 17 are patentable over Wilson. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226/076001).

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Respectfully submitted,

By _____

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